FIG. 1

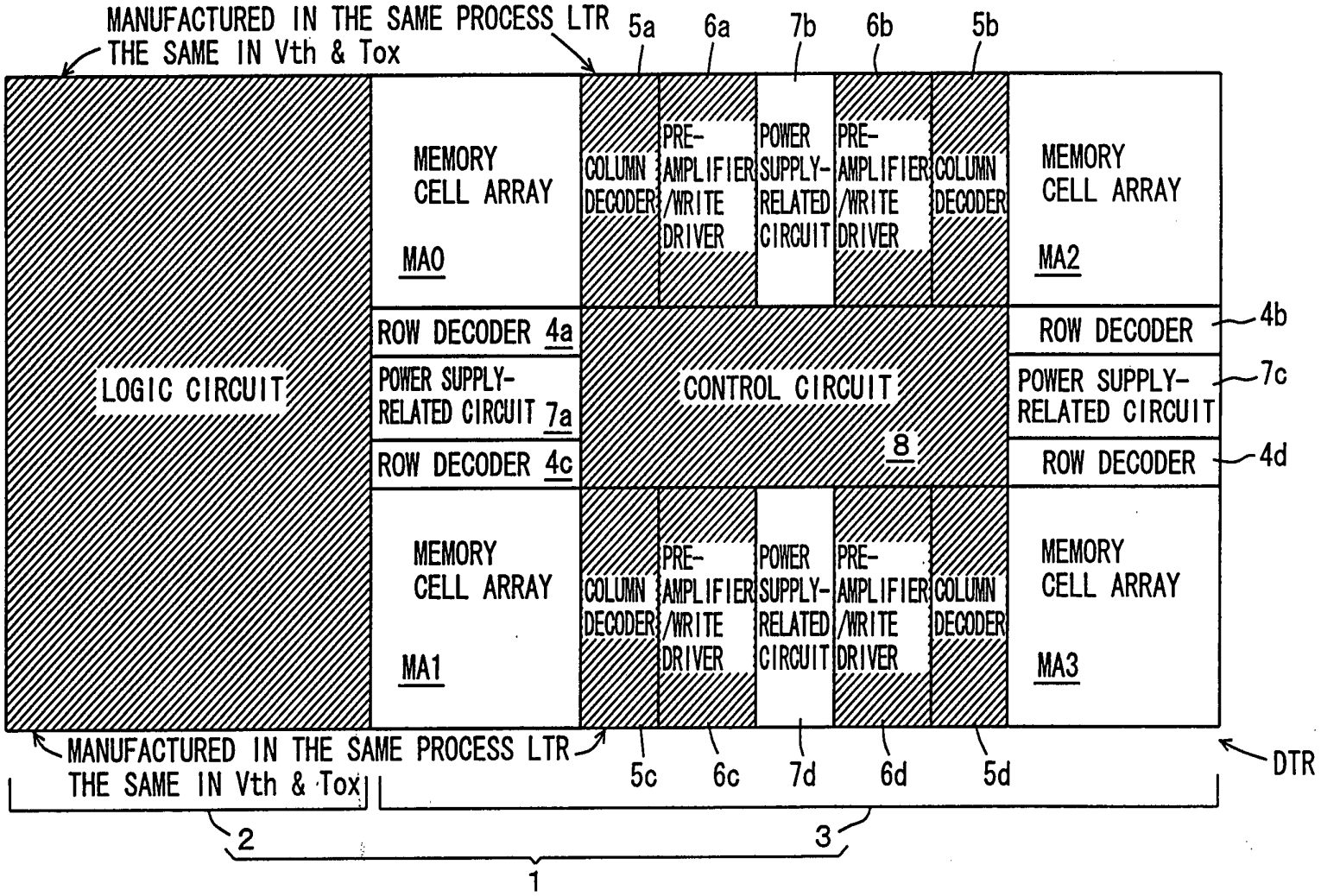

MANUFACTURED IN THE SAME PROCESS LTR
THE SAME IN Vth & Tox
5a
6a
7b
6b
5b
LOGIC CIRCUIT
MEMORY CELL ARRAY
MA0
COLUMN DECODER
PRE-AMPLIFIER /WRITE DRIVER
POWER SUPPLY-RELATED CIRCUIT
PRE-AMPLIFIER /WRITE DRIVER
COLUMN DECODER
MEMORY CELL ARRAY
MA2
ROW DECODER 4a
ROW DECODER
4b
POWER SUPPLY-RELATED CIRCUIT 7a
CONTROL CIRCUIT
8
POWER SUPPLY-RELATED CIRCUIT
7c
ROW DECODER 4c
ROW DECODER
4d
MEMORY CELL ARRAY
MA1
COLUMN DECODER
PRE-AMPLIFIER /WRITE DRIVER
POWER SUPPLY-RELATED CIRCUIT
PRE-AMPLIFIER /WRITE DRIVER
COLUMN DECODER
MEMORY CELL ARRAY
MA3
MANUFACTURED IN THE SAME PROCESS LTR
THE SAME IN Vth & Tox
5c
6c
7d
6d
5d
DTR
2
3
1

FIG. 2

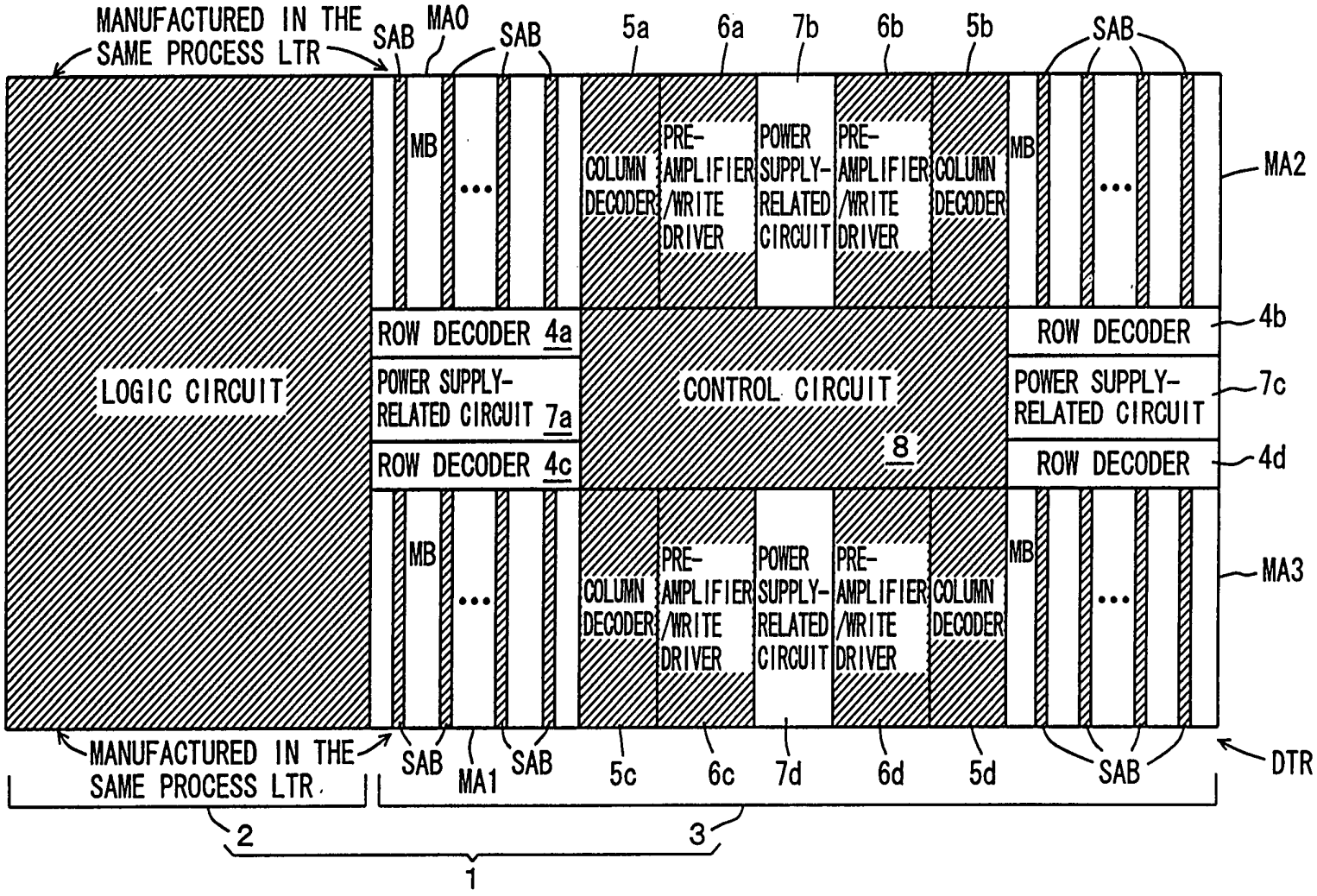

MANUFACTURED IN THE SAME PROCESS LTR
SAB
MA0
SAB
5a
6a
7b
6b
5b
SAB
MB
COLUMN DECODER
PRE-AMPLIFIER /WRITE DRIVER
POWER SUPPLY-RELATED CIRCUIT
PRE-AMPLIFIER /WRITE DRIVER
COLUMN DECODER
MB
MA2
ROW DECODER 4a
ROW DECODER
4b
LOGIC CIRCUIT
POWER SUPPLY-RELATED CIRCUIT 7a
CONTROL CIRCUIT
8
POWER SUPPLY-RELATED CIRCUIT
7c
ROW DECODER 4c
ROW DECODER
4d
MB
COLUMN DECODER
PRE-AMPLIFIER /WRITE DRIVER
POWER SUPPLY-RELATED CIRCUIT
PRE-AMPLIFIER /WRITE DRIVER
COLUMN DECODER
MB
MA3
MANUFACTURED IN THE SAME PROCESS LTR
SAB
MA1
SAB
5c
6c
7d
6d
5d
SAB
DTR
2
3
1

FIG. 3

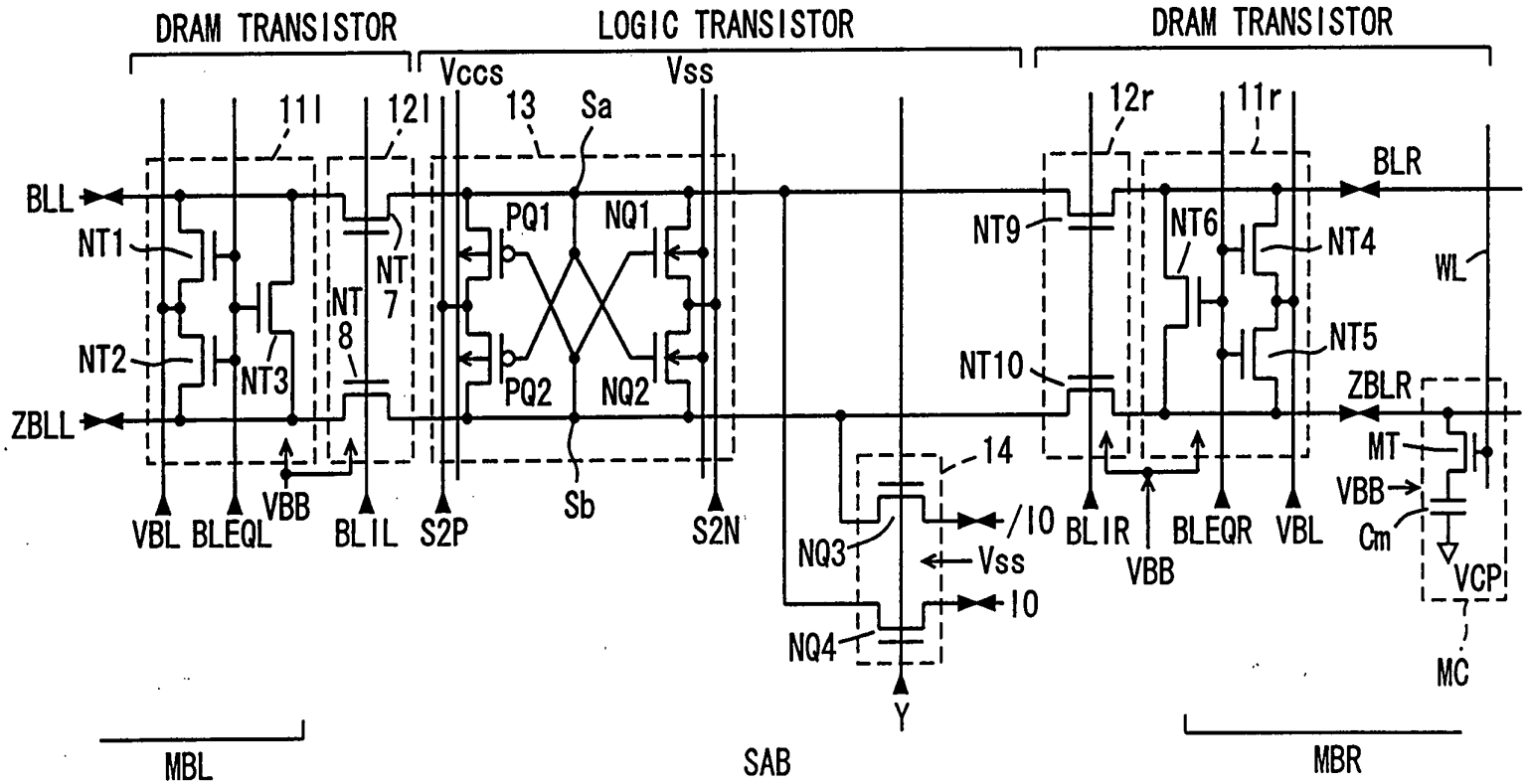

DRAM TRANSISTOR
LOGIC TRANSISTOR
DRAM TRANSISTOR
Vccs
Vss
11l
12l
13
Sa
12r
11r
BLL
BLR
NT1
NT2
NT3
NT 7
NT 8
PQ1
PQ2
NQ1
NQ2
NT9
NT10
NT6
NT4
NT5
WL
ZBLL
ZBLR
MT
VBB
Cm
VCP
MC
VBL
BLEQL
BLIL
S2P
Sb
S2N
14
/IO
Vss
IO
NQ3
NQ4
Y
BLIR
BLEQR
VBL
VBB
MBL
SAB
MBR

FIG. 4

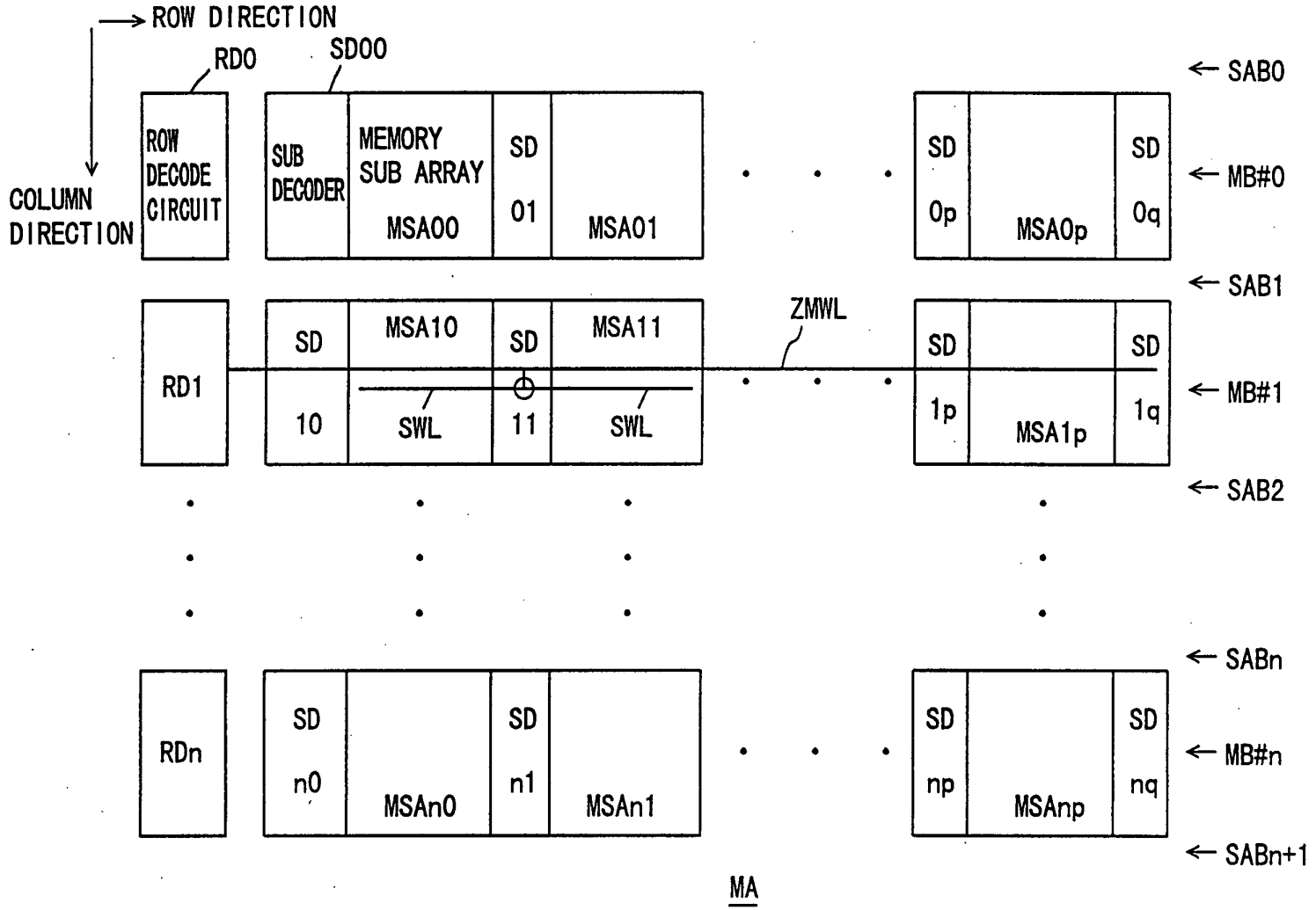

ROW DIRECTION
COLUMN DIRECTION
RD0
SD00
ROW DECODE CIRCUIT
SUB DECODER
MEMORY SUB ARRAY
MSA00
SD 01
MSA01
SD 0p
MSA0p
SD 0q
SAB0
MB#0
SAB1
RD1
SD 10
MSA10
SWL
SD 11
MSA11
SWL
ZMWL
SD 1p
MSA1p
SD 1q
MB#1
SAB2
RDn
SD n0
MSAn0
SD n1
MSAn1
SD np
MSAnp
SD nq
SABn
MB#n
SABn+1
MA

FIG. 5

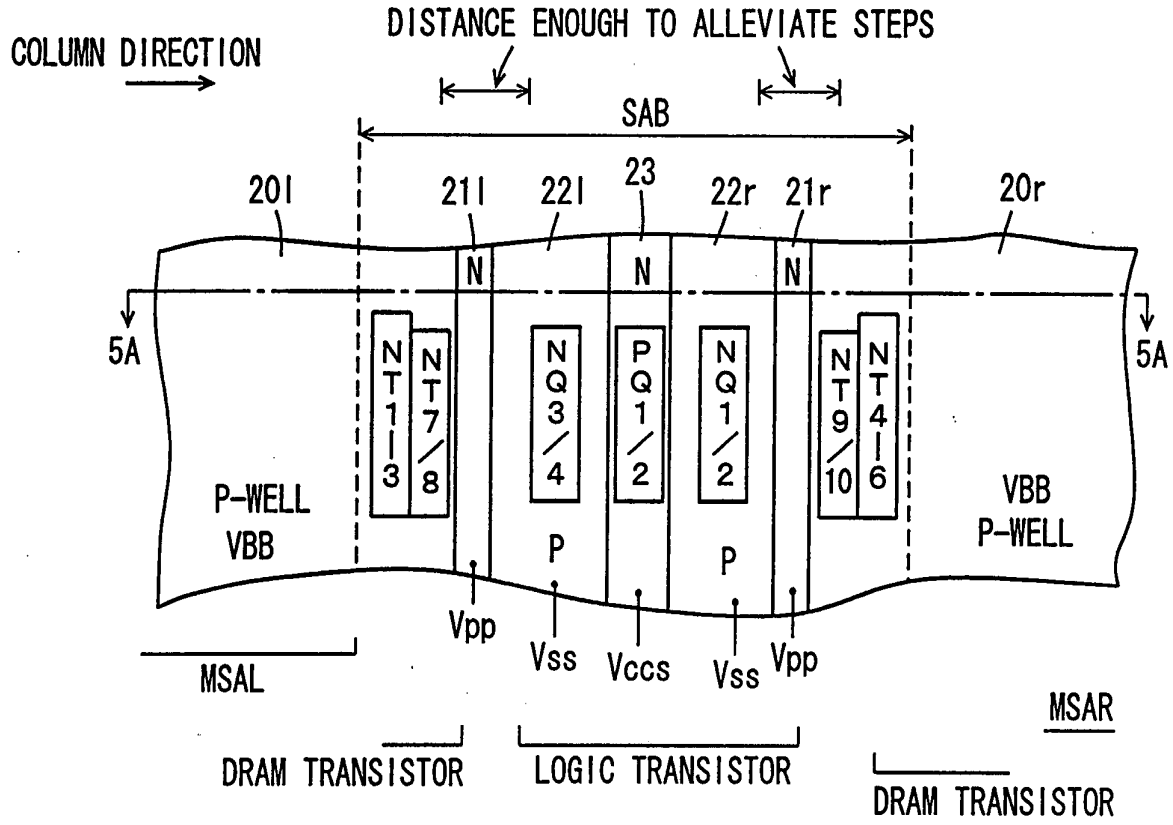

COLUMN DIRECTION
DISTANCE ENOUGH TO ALLEVIATE STEPS
SAB
20l
21l
22l
23
22r
21r
20r
N
N
N
5A
5A
NT1/3
NT7/8
NQ3/4
PQ1/2
NQ1/2
NT9/10
NT4/6
P-WELL
VBB
VBB
P-WELL
P
P
Vpp
Vss
Vccs
Vss
Vpp
MSAL
MSAR
DRAM TRANSISTOR
LOGIC TRANSISTOR
DRAM TRANSISTOR

FIG. 6

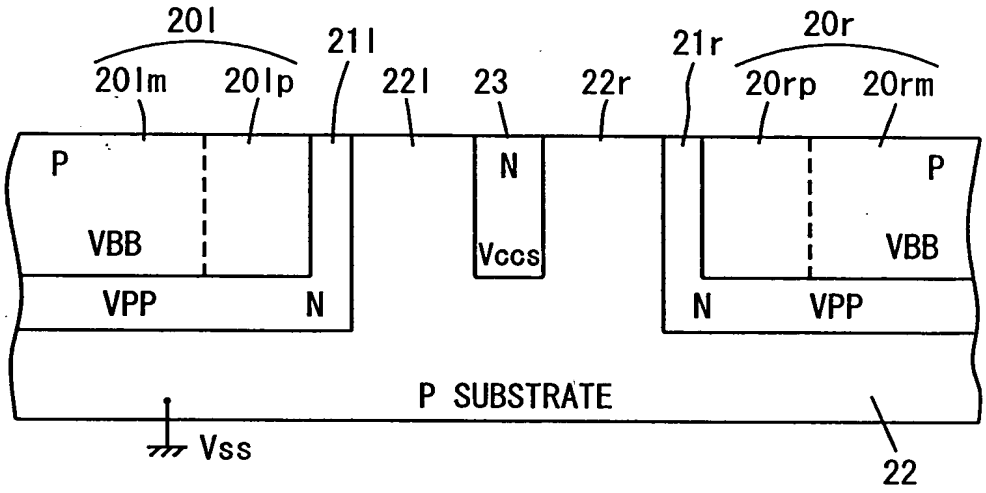

20l
21l
21r
20r
20lm
20lp
22l
23
22r
20rp
20rm
P
N
P
VBB
Vccs
VBB
VPP
N
N
VPP
P SUBSTRATE
Vss
22

FIG. 7

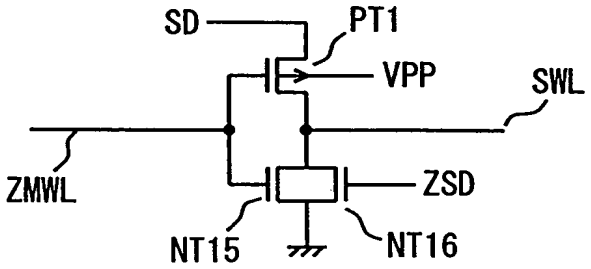

SD
PT1
VPP
SWL
ZMWL
ZSD
NT15
NT16

FIG. 8

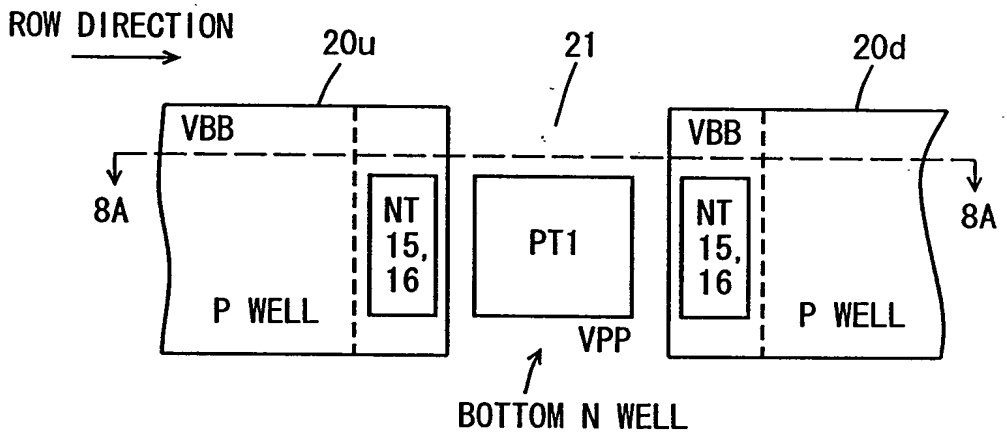

ROW DIRECTION
20u
21
20d
VBB
VBB
8A
8A
NT
15,
16
PT1
NT
15,
16
P WELL
VPP
P WELL
BOTTOM N WELL

FIG. 9

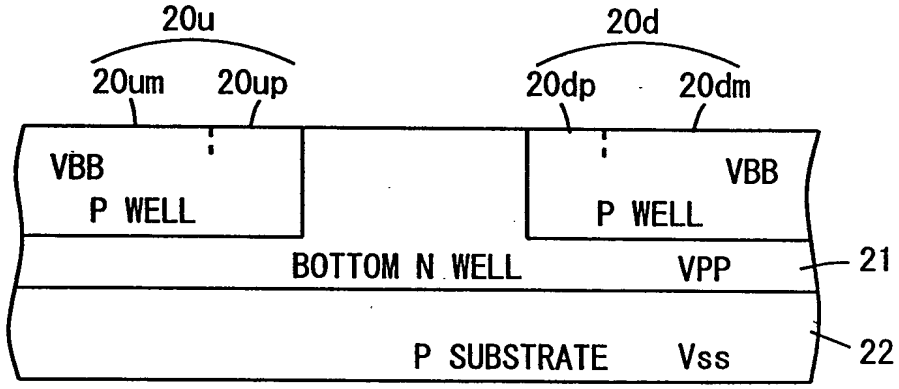

20u
20d
20um
20up
20dp
20dm
VBB
P WELL
VBB
P WELL
BOTTOM N WELL
VPP
21
P SUBSTRATE
Vss
22

FIG. 10

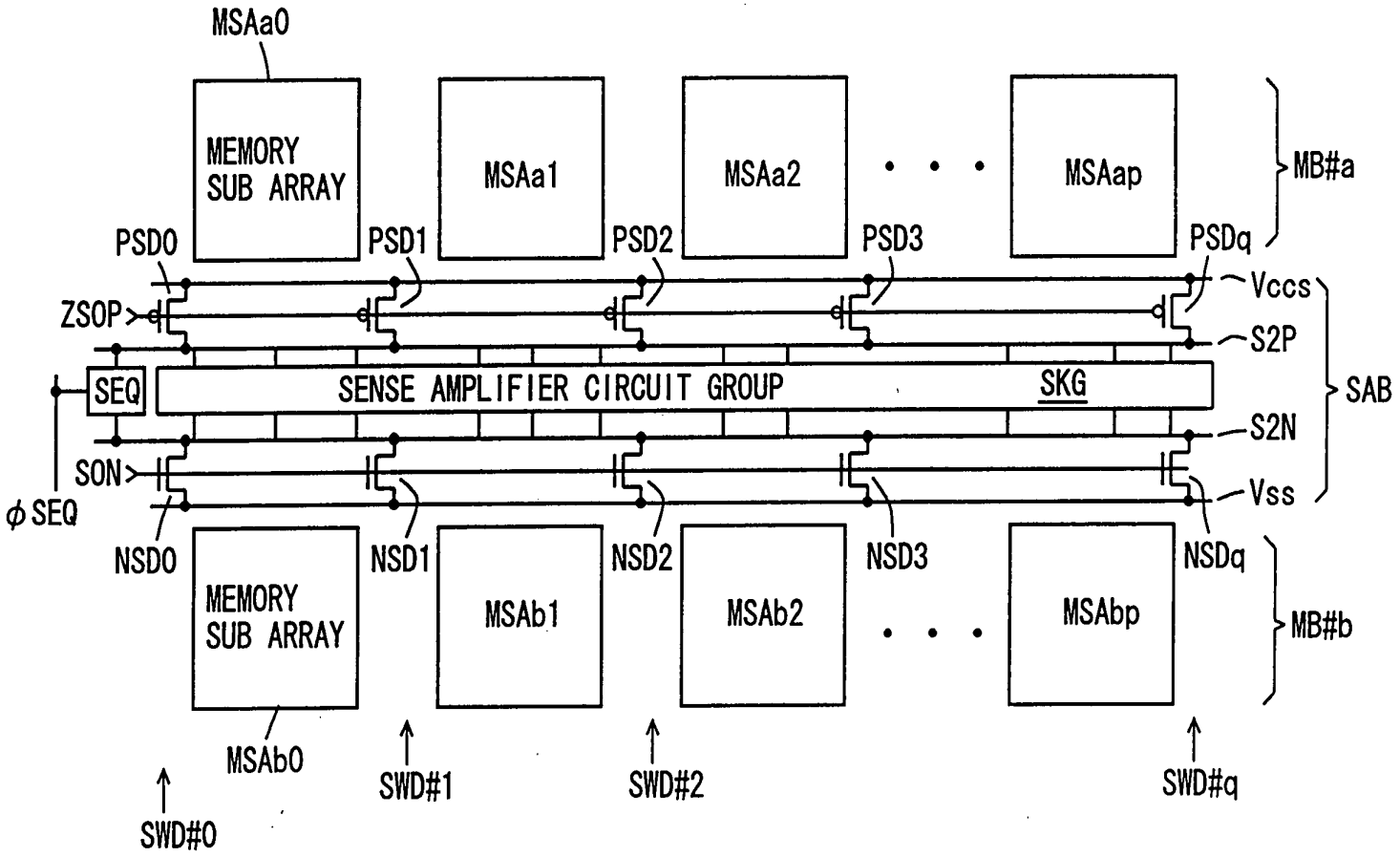

MSAa0
MEMORY SUB ARRAY
MSAa1
MSAa2
MSAap
MB#a
PSD0
PSD1
PSD2
PSD3
PSDq
ZSOP
Vccs
S2P
SEQ
SENSE AMPLIFIER CIRCUIT GROUP
SKG
SAB
S2N
SON
Vss
φSEQ
NSD0
NSD1
NSD2
NSD3
NSDq
MEMORY SUB ARRAY
MSAb1
MSAb2
MSAbp
MB#b
MSAb0
SWD#1
SWD#2
SWD#q
SWD#0

FIG. 11

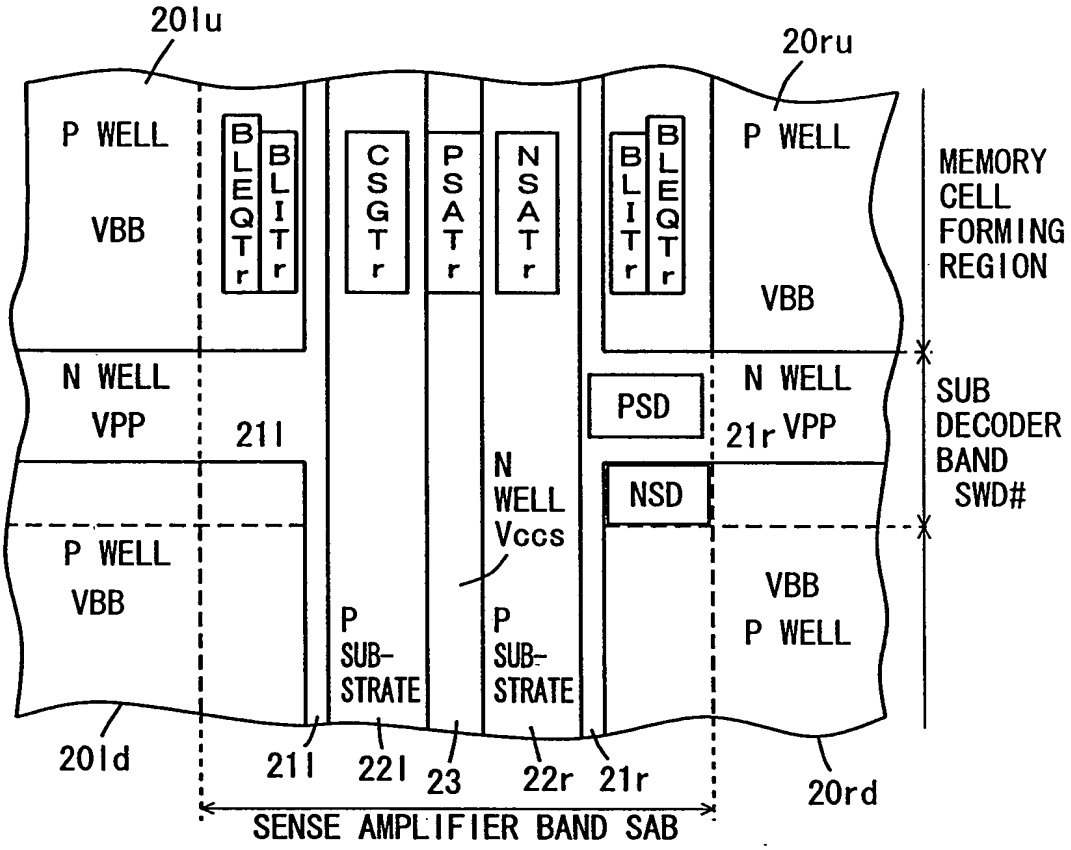

20lu
20ru
P WELL
VBB
BLEQTr
BLITr
CSGTr
PSATr
NSATr
BLITr
BLEQTr
P WELL
VBB
MEMORY CELL FORMING REGION
N WELL
VPP
211
PSD
N WELL
21r VPP
SUB DECODER BAND SWD#
N WELL Vccs
NSD
P WELL
VBB
P SUB-STRATE
P SUB-STRATE
VBB
P WELL
20ld
211
221
23
22r
21r
20rd
SENSE AMPLIFIER BAND SAB

FIG. 12

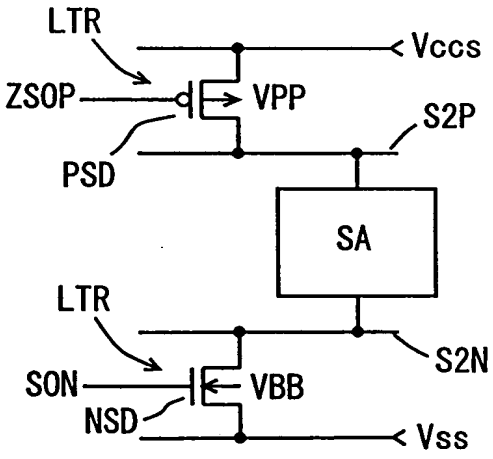

LTR
Vccs
ZSOP
VPP
S2P
PSD
SA
LTR
S2N
SON
VBB
NSD
Vss

FIG. 13

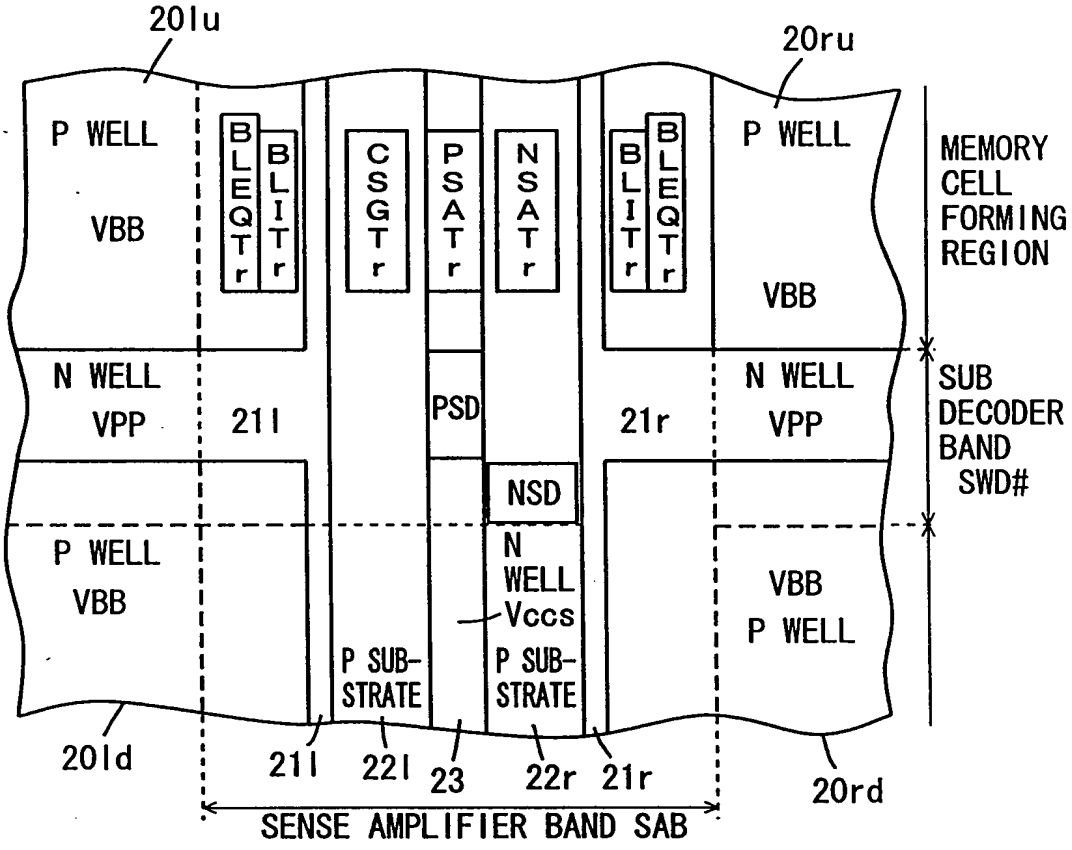

20lu
20ru
P WELL
VBB
BLEQTr
BLITr
CSGTr
PSATr
NSATr
BLITr
BLEQTr
P WELL
VBB
MEMORY CELL FORMING REGION
N WELL
VPP
21l
PSD
21r
N WELL
VPP
SUB DECODER BAND SWD#
NSD
P WELL
VBB
N WELL
Vccs
VBB
P WELL
P SUB-STRATE
P SUB-STRATE
20ld
21l
22l
23
22r
21r
20rd
SENSE AMPLIFIER BAND SAB

FIG. 14

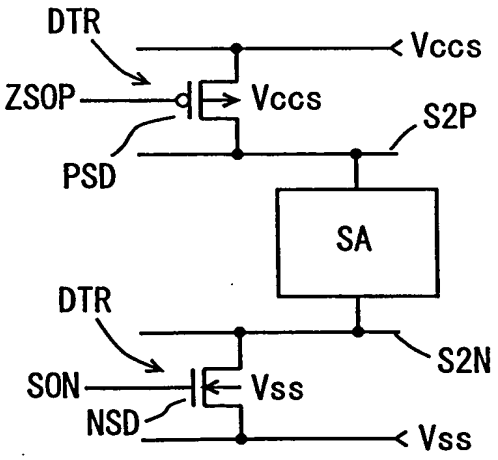

DTR
Vccs
ZSOP
Vccs
S2P
PSD
SA
DTR
S2N
SON
Vss
NSD
Vss

FIG. 15

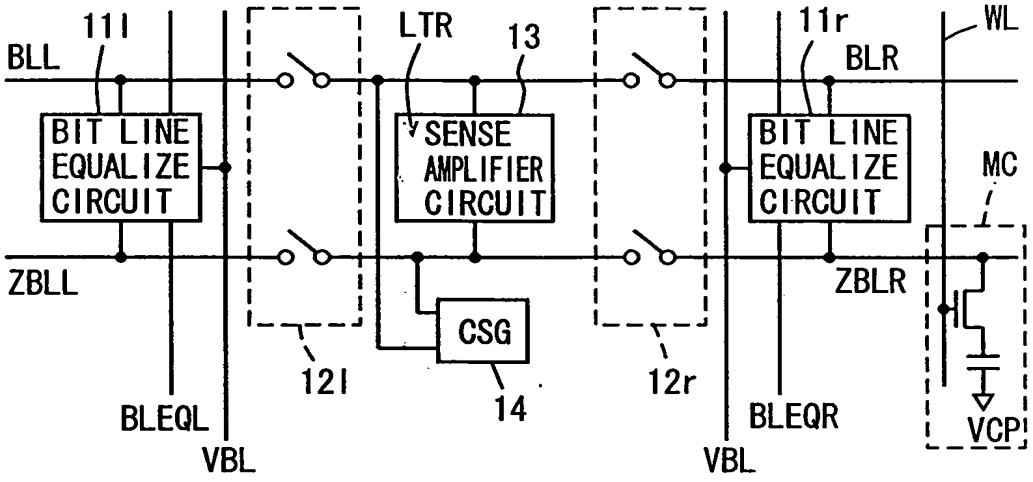

BLL
11l
LTR
13
11r
BLR
WL
BIT LINE EQUALIZE CIRCUIT
SENSE AMPLIFIER CIRCUIT
BIT LINE EQUALIZE CIRCUIT
MC
ZBLL
ZBLR
CSG
12l
12r
14
BLEQL
VBL
VBL
BLEQR
VCP

FIG. 16

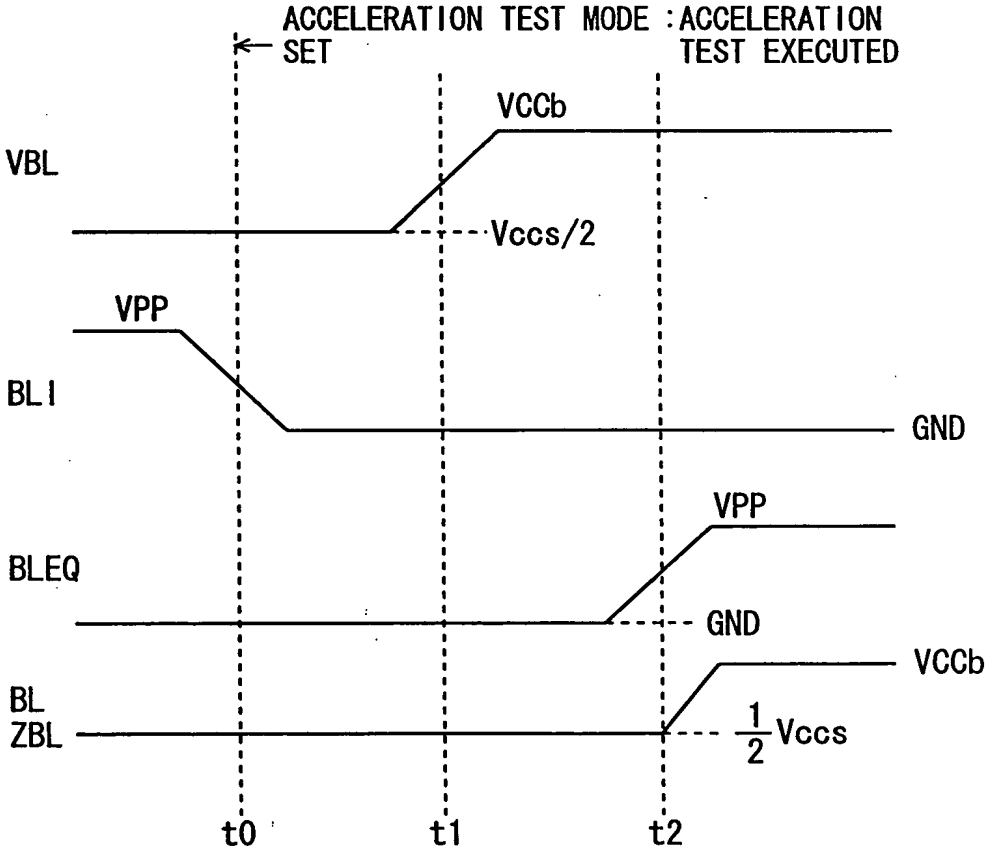

ACCELERATION TEST MODE SET
ACCELERATION TEST EXECUTED
VCCb
VBL
Vccs/2
VPP
BLI
GND
VPP
BLEQ
GND
VCCb
BL
ZBL
1/2 Vccs
t0
t1
t2

FIG. 17

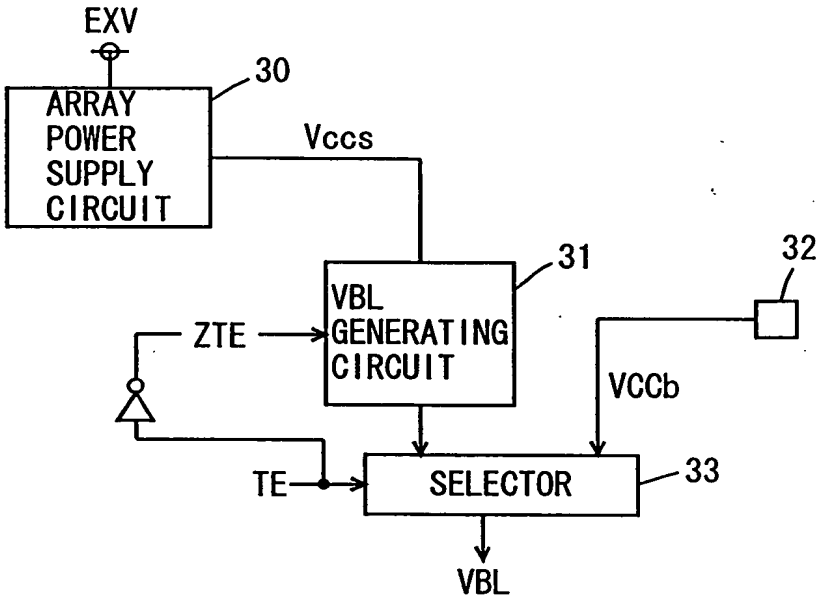


FIG. 18

FIG. 19

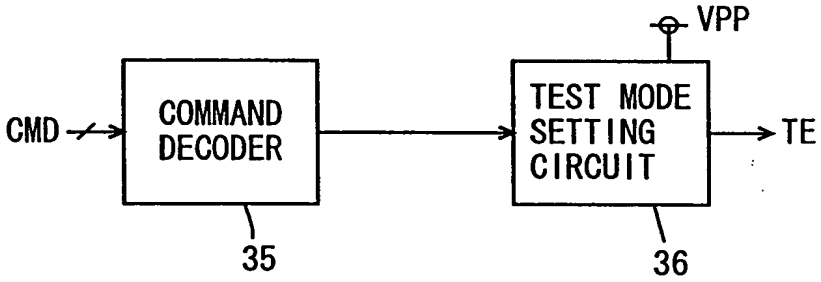


FIG. 20

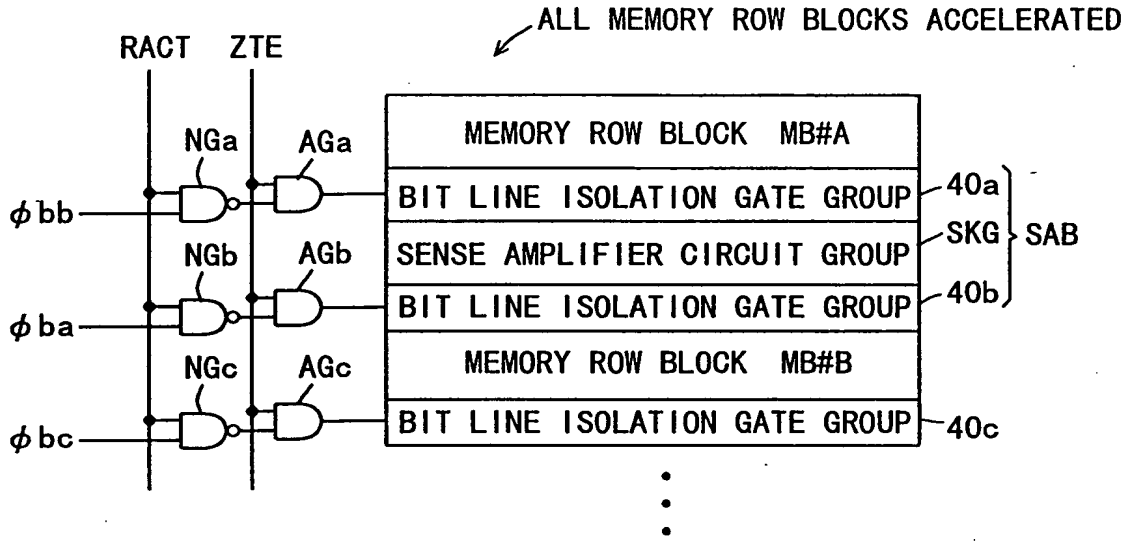


FIG. 21

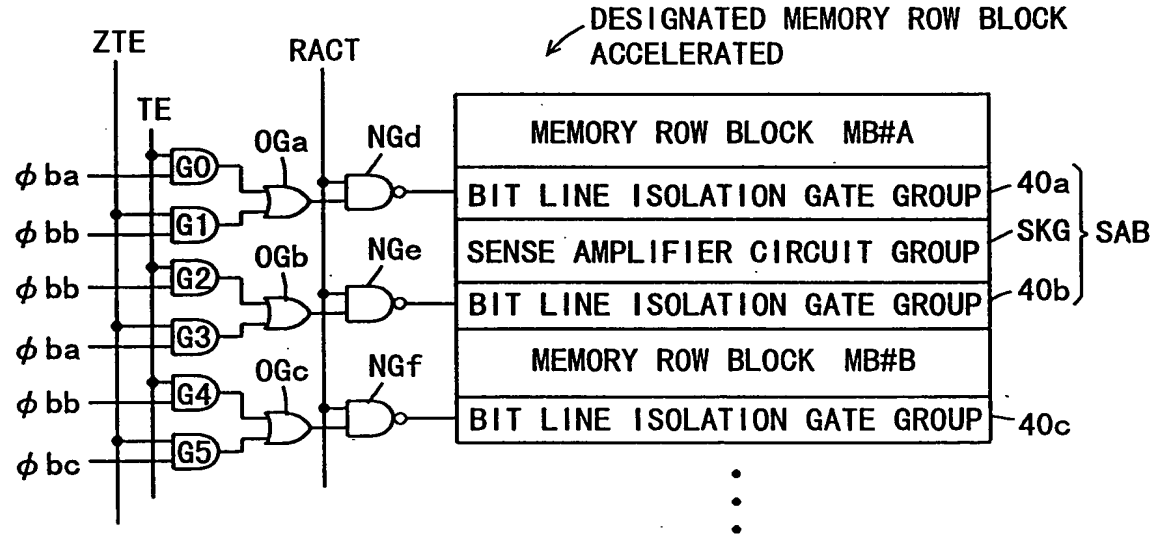


FIG. 22

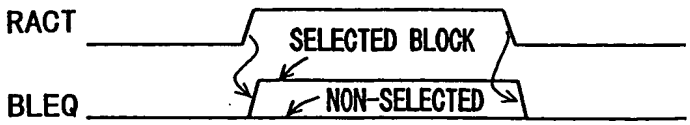


FIG. 23A

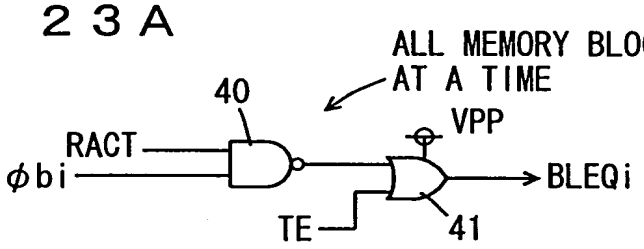


FIG. 23B

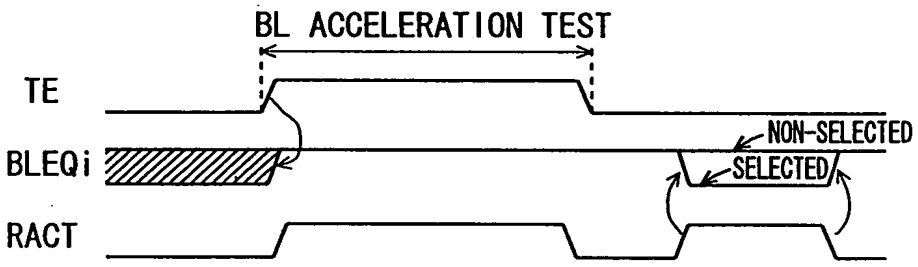


FIG. 24

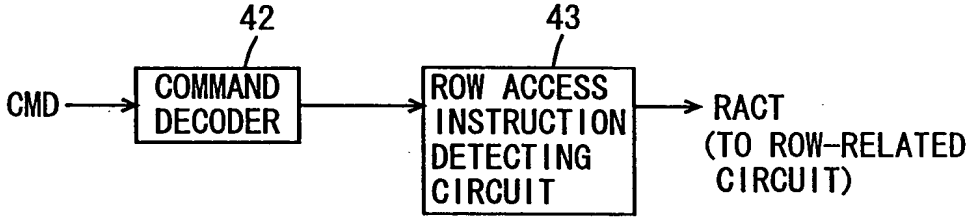


FIG. 25A

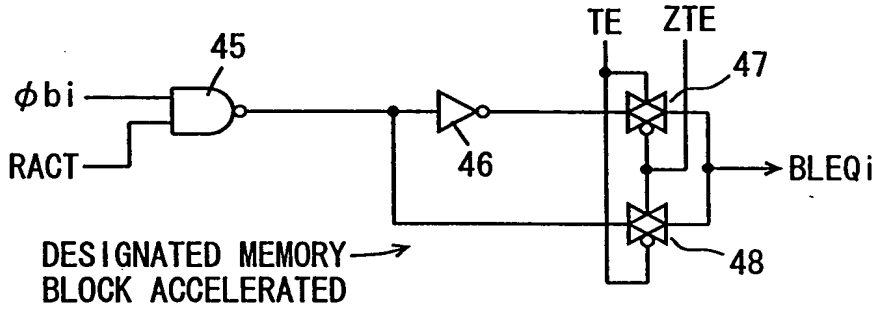


FIG. 25B

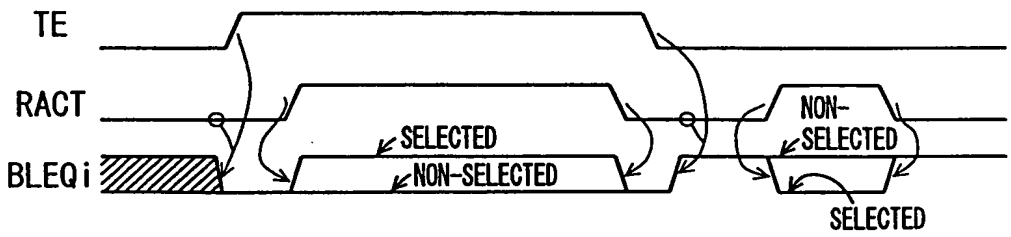


FIG. 26 PRIOR ART

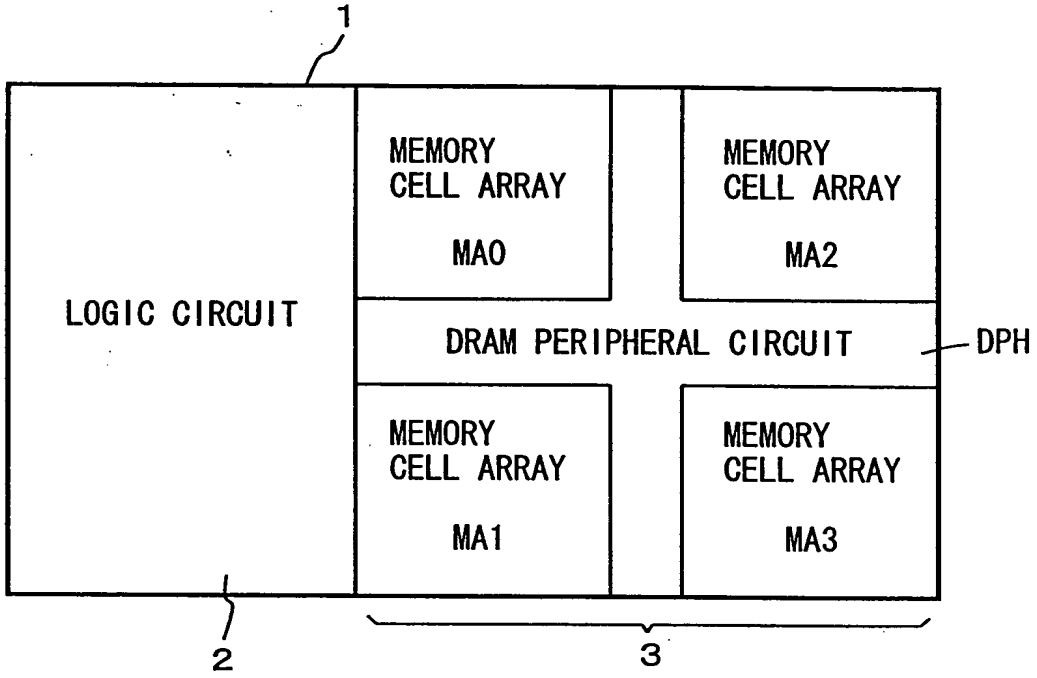
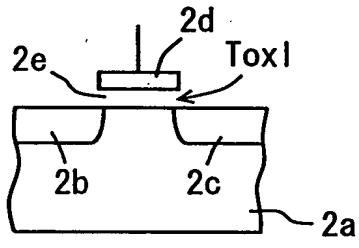
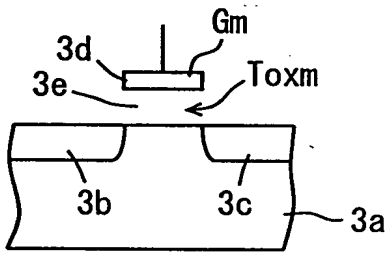


FIG. 27A PRIOR ART



LTR
Low - Vth

FIG. 27B PRIOR ART



DTR
M - Vth
Toxm > Toxl